LH77790

Embedded Microcontroller

DESCRIPTION

The LH77790 Embedded microcontroller is an ARM7D-based system on chip with a high level of integration. In addition to the CPU, it consists of a number of essential peripherals, instruction/data cache, and Static RAM. The target applications are handheld, battery operated devices that require performance greater than that available from 16-bit and 32-bit CISC-based controllers. These devices include all monochrome LCD displays, keyboards, non-volatile memory (typically Flash), Static RAM, and other communications ports and external peripherals. The Embedded controller provides the features required in these systems, including an LCD controller, no-glue memory (SRAM / DRAM / EEPROM / Flash) interface, and other peripherals that eliminate all external components, except for memory and buffers (i.e. RS232 level converters). The LH77790 allows an external bus master to take control of the external as well as the internal interface (address bus, data bus, controls).

FEATURES

- Highly integrated single chip
- 32-bit ARM7D CPU core
- 2 kB (B : byte) data/instruction cache
- 2 kB Static RAM (4 kB without cache)
- Low power
- High performance
- Programmable clock and power management
- Programmable monochrome LCD controller
- On-chip interrupt controller
- Three UARTs - 16C450-class
- IrDA/DASK infrared interface
- Three pulse width modulator channels
- Simplified no glue memory interface
- On-chip DRAM controller
- 24-bit Programmable Peripheral Interface (PPI)
- Three 16-bit counter/timer channels
- Hardware watchdog timer
- Dual range operation
  5 V TTL/25 MHz
  3.3 V LVTTL/16.7 MHz
- Package : 176-pin LQFP (LQFP176-P-2424)

APPLICATIONS

- Hand-held personal equipment (GPSs, PDAs, communications, games)
- Point-of-sale (barcode scanners, portable inventory controllers)
- Industrial instrumentation (portable oscilloscopes, analyzers)

DEVELOPMENT TOOLS

The ARM software development toolkit provides a complete integrated environment for software development. The toolkit provides a complete toolset for :

- Software simulation via ARMulator
- ANSI C optimized compiler
- ARM assembler

The ARM software development toolkit is available on the following platforms :

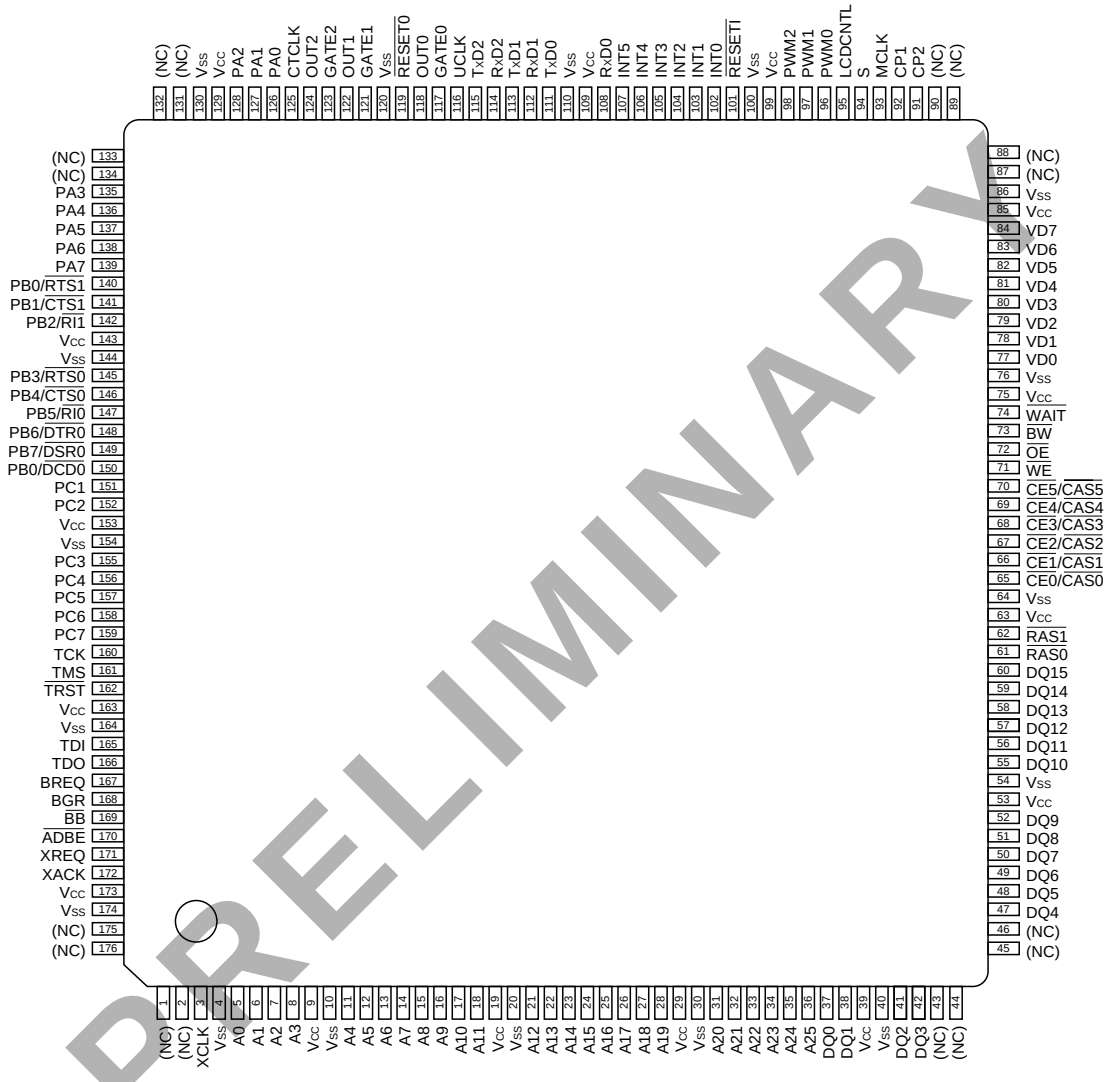
- Windows 95
- Windows 3.1x
- Windows NT (Intel and Alpha)
- MS DOS 6.x
- Sun Os 4.1x

ARM POWERED

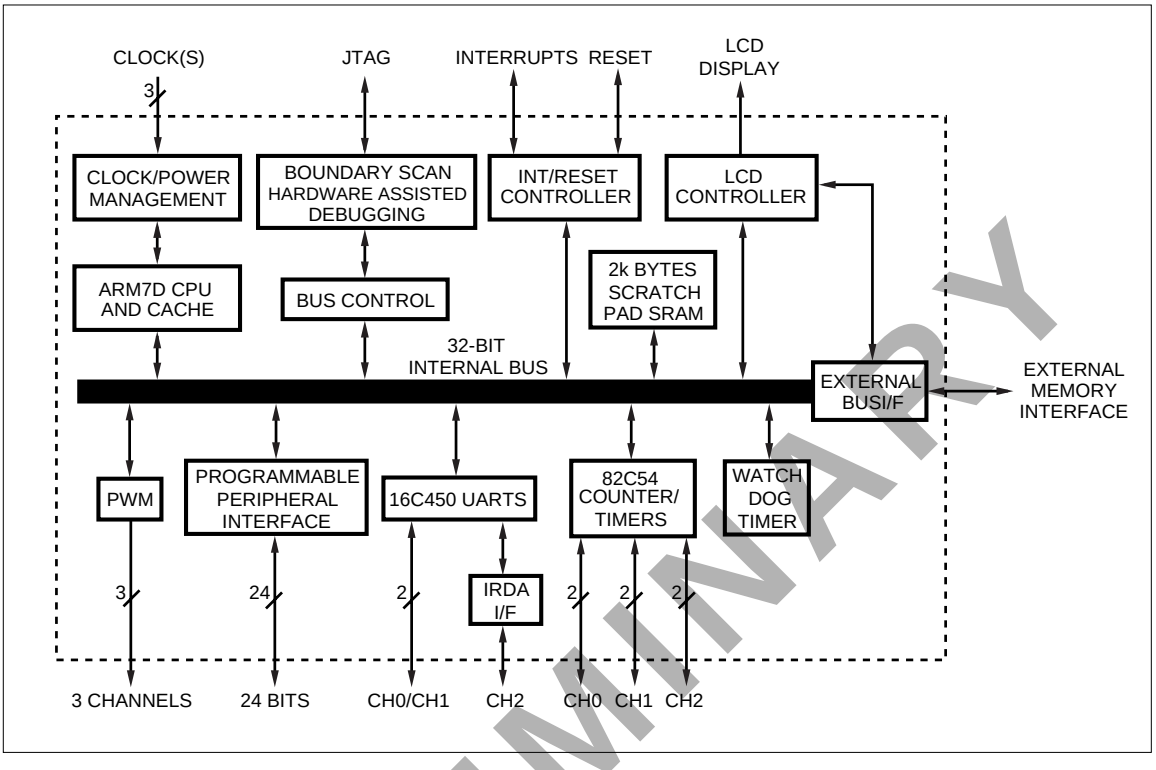
TM

PIN CONNECTIONS

176-PIN LQFP TOP VIEW



BLOCK DIAGRAM



PIN DESCRIPTION

PIN NAME	OPERATIONAL MODE#		DESCRIPTION
	MASTER	SLAVE	
EXTERNAL BUS INTERFACE			
A[25:0]*	O	I	**Master mode :** External address bus. The Embedded microcontroller will provide a 26-bit address to external memories and peripherals. **Slave mode :** External address bus. The external bus master will provide a 26-bit address to the Embedded microcontroller. The High order six bits of the address are provided by an internal programmable register giving the external bus master full access a 32-bit address space. The Embedded microcontroller tristates the address bus in slave mode.
DQ[15:0]*	I/O	I/O	External 16-bit data bus. The Embedded microcontroller tristates the data bus in slave mode.
$\overline{OE}$*	O	I	**Master mode :** Output enable for external memory and peripherals. $\overline{OE}$ allows external memory and peripherals to drive the data bus and is asserted Low during a read operation. **Slave mode :** Output enable for Embedded microcontroller. $\overline{OE}$ should be driven Low during a read operation by the external bus master. The Embedded microcontroller tristates $\overline{OE}$ in slave mode.
$\overline{WE}$*	O	I	**Master mode :** Write enable for external memory and peripherals. During a write operation, this pin is driven Low. During a read operation, this pin is driven High. **Slave mode :** Determines the direction data transfer. Low indicates a write operation (External bus master --> Embedded microcontroller) and High indicates a read operation (Embedded microcontroller --> External bus master). The Embedded microcontroller tristates $\overline{WE}$ in slave mode.
$\overline{CE}$[5:0]/ $\overline{CAS}$[5:0]	O	O	These pins provide the chip enables/column address select to directly connect to standard external memory/peripheral devices. The pins act as $\overline{CAS}$ when interfacing to DRAMs and $\overline{CE}$ otherwise. They are fully programmable by the system designer and can support byte enables.
$\overline{RAS}$[1:0]	O	O	Row address select pins for DRAM Bank 0 and Bank 1. Embedded microcontroller refreshes the external DRAM in both master and slave modes.
$\overline{WAIT}$	I	I	External memory wait. Allows the use of slow memories.
$\overline{BW}$*	O	I	**Master mode :** Byte wide access. The ARM-CPU indicates to external memory and peripherals the data size of the data transfer. When Low, the data transfer is a byte length. Can be used by an external address decoder to generate extra chip/byte enables. **Slave mode :** Size transfer. The external bus master indicates the transfer size. Low indicates a byte transfer and High indicates a halfword transfer. The Embedded microcontroller tristates $\overline{BW}$ in slave mode.

$\overline{BB}$	I	O	**Master mode :** Byte boot selects between x 8 or x 16 for the boot memory. It is sampled when $\overline{RESETI}$ transitions from Low to High. **Slave mode :** The external bus master can provide its own address to the Embedded microcontroller on the address bus in which case this pin should be Low. The external bus master can also use an internal counter to the Embedded microcontroller as an address source in which case this pin should be High. In slave mode, the High order six bits of the address are provided by an internal programmable register.
BREQ	I	I	Bus master request. An external bus master can request control of the external as well as internal interfaces (data bus, address bus, controls) by asserting this pin High. When the Embedded microcontroller is ready to release the interface, it will drive High BGR. By asserting BREQ Low, the external bus controller indicates to the Embedded microcontroller it is releasing the interface.
BGR	O	O	Bus master grant. Upon detecting BREQ = High, the Embedded microcontroller grants and allows the external bus master to take control of the external as well as internal interfaces by asserting this pin High, and releasing the data bus, address bus and controls. The Embedded microcontroller will operate in slave mode. The external bus master has control as long as BGR is driven High. In slave mode, the Embedded microcontroller will continue to refresh the DRAM banks as programmed. The Embedded Microcontroller can takeover (operate in master mode) the interface by asserting BGR Low.
XREQ	I	I	**Master mode :** No function **Slave mode :** Transfer request. The external bus master can request access the Embedded microcontroller internal SRAM, cache, registers, DRAM controller, or SRAM controller by asserting this pin High during BFR = High, and providing address, data, and controls as necessary. Burst access is not supported.
XACK	O	O	Transfer acknowledge. Upon detecting XREQ = High, the Embedded microcontroller acknowledges the transfer request by asserting XACK High, latching address, data, and controls. The Embedded microcontroller will take control of the interface by asserting BGR Low. Upon completing the transfer, the Embedded microcontroller will drive XACK Low, drive the data bus on a read operation and continue to assert BGR Low as long as XREQ is High. When XREQ is driven Low, the Embedded microcontroller asserts BGR High giving the external bus master control of the interface.
COUNTERS/TIMERS INTERFACE			
GATE[2:0]	I	I	Counter/timer control gate input signals.
OUT[2:0]	O	O	Counter/timer output signals may be connected to interrupt input signals.
INTERRUPT INTERFACE			
INT[5:0]	I	I	External interrupt input signals.

LCD CONTROLLER INTERFACE			
CP_2	O	O	Display data shift clock to LCD display.
CP_1	O	O	Display data latch pulse and scan signal transfer clock signal.
MCLK	O	O	LCD display frame signal.
S	O	O	Scan line start pulse to LCD display.
LCDCNTL	O	O	LCDC output control to LCD.
VD[7:0]	O	O	Video data to LCD display.
PROGRAMMABLE PERIPHERAL INTERFACE			
PA[7:0], PB[7:0], PC[7:0]	I/O	I/O	Parallel ports A, B, and C signals. Signals have programmable operation and can function as input, output or controls. PB[7:0] and PC0 are multiplexed with UART's MODEM signals.
PWM INTERFACE			
PWM[2:0]	O	O	Pulse width modulator output signals.
UARTS INTERFACE			
RxD[2:0]	I	I	UART serial data input signals. RxD2 also doubles as the digital input for the IrDA interface.
TxD[2:0]	O	O	UART serial data output signals. TxD2 also doubles as the digital output for the IrDA interface.
$\overline{RTS}$[1:0]	O	O	Request to send for UARTs 0 & 1. Multiplexed with PB0 & PB3 respectively.
$\overline{CTS}$[1:0]	I	I	Clear to send for UARTs 0 & 1. Multiplexed with PB1 & PB4 respectively.
$\overline{RI}$[1:0]	I	I	Ring indicator for UARTs 0 & 1. Multiplexed with PB2 & PB5 respectively.
$\overline{DTR_0}$	O	O	Data terminal ready for UART 0 only. Multiplexed with PB6.
$\overline{DSR_0}$	I	I	Data set ready for UART 0 only. Multiplexed with PB7.
$\overline{DCD_0}$	I	I	Data carrier detect for UART 0 only. Multiplexed with PC0.
RESET & EXTERNAL CLOCKS			
$\overline{RESETI}$	I	I	Chip reset input. It should be driven Low for at least 6 cycles to guarantee a proper reset. $\overline{RESETI}$ has a built-in glitch detector. $\overline{RESETO}$ will be driven Low after a valid reset is detected for as long as $\overline{RESETI}$ is driven Low.
$\overline{RESETO}$	O	O	Chip reset output. It will be driven Low during : (1) Chip reset (2) WDT timeout reset (8 cycles) (3) Software controlled reset
XCLK	I	I	The Embedded microcontroller external clock input pin.
UCLK	I	I	UART/DASK demodulator external clock input signal.
CTCLK	I	I	Counter/timer external clock input signal.
JTAG INTERFACE			
TCK	I	I	JTAG test clock input signal. This pin is not part of the scan chain.
TMS	I	I	JTAG test mode select input signal. This pin is not part of the scan chain.
$\overline{TRST}$	I	I	JTAG test scan reset input. This pin is not part of the scan chain.
TDI	I	I	JTAG test data input signal. This pin is not part of the scan chain.
TDO	O	O	JTAG test data output signal. This pin is not part of the scan chain.

TEST INTERFACE			
$\overline{\text{ADBE}}$	I	I	Test Pin. For normal operation, this pin should be High. This pin is not part of the scan chain

N/A : Not Available

Master mode : The Embedded microcontroller is the bus master (BGR = 0)

Slave mode : An external device is the bus master (BGR = 1)

*Tristated in slave mode

FUNCTIONAL DESCRIPTION

CPU Core

The CPU core is the ARM7D. The ARM7D is comprised of the ARM7 processor, with Debugging (D) features provided with access via the JTAG test port.

FEATURES

- ARM7D 32-bit RISC CPU
- Low power consumption
- High performance
- Fast interrupt response with minimal context switching
- 25 MHz at 5 V, 16.7 MHz at 3.3 V
- Excellent High-level language support
- Simple but powerful instruction set
- Little endian operation mode
- Fully static design for power sensitive applications

Cache

The 2 kB on-chip cache provides for zero wait state operation on cache hits. It is a combined data/instruction cache.

FEATURES

- 2 kB cache
- 4-way associative
- Line size = 1 word, 128 sets
- Combined instruction/data
- Write-Back Policy
- Least recently used replacement policy
- Four modes of operation :
  - 2 kB cache
  - 3.625 kB SRAM (giving a total of 5.625 kB local SRAM) mode
  - Flush mode
  - Invalidate mode

Local SRAM

The 2 kB local SRAM provides zero wait state operation and is ideal for fast access to critical data or code (such as interrupt service routines).

FEATURES

- 2 kB expandable to 5.625 kB (See Cache section)
- Read/write programmable

Memory and Peripheral Interface

The Embedded microcontroller supports standard x 8 and x 16 SRAM, DRAM, EEPROM, and Flash memory devices. It also supports memory mapped peripherals through a programmable external bus controller with little or no glue logic, resulting in lower power consumption and cost savings in device count and board area.

FEATURES

- Supports 26-bit address bus
- Supports 16-bit data bus
- Memory management
- SRAM controller
  - Six SRAM banks
- DRAM controllers
  - Two DRAM banks
- Programmable properties :
  - Six multiplexed chip enables/$\overline{\text{CAS}}$ pins
  - Two RAS pins
  - 0-7 wait states
  - 8/16-bit bus width
  - Half word access
  - Access privilege for user/system
- External memory mapped I/O support
- LCD frame buffer support

Memory Management

The ARM CPU can address up to 4 GB of address space (32-bit internal address). The Embedded microcontroller can address up to 64 MB (26-bit external address). The Embedded microcontroller supports up to eight programmable segments (0-7). Each segment can address 64 MB of external memory. This will give a total of 512 MB external addressable space.

FEATURES

- Supports eight programmable segments
- Supports one default segment
- Each segment consists of :
  - START register
  - STOP register
  - Segment descriptor register (SDR)
- SDR contains information on :
  - System/user privileges
  - Cacheability
  - Cache write policy
  - 16/32-bit mode
  - Memory bank selection
- Supports eight memory banks
  - Six SRAM banks and two DRAM banks
  - Each bank has a bank configuration register (BCR)
  - BCRs reflect external memory properties

Logical to Physical Mapping

When the external bus controller receives an internal address for a memory access, it maps the address to the appropriate segment (or default segment) and performs all the necessary check for cacheability and privileges as programmed in the SDR. Once all the checks are passed, the external bus controller accesses the appropriate memory bank, BCR, as programmed in the SER. BCR tells the external bus controller which external device to select and its properties. The lower 26 bits of the address are used to address the external device.

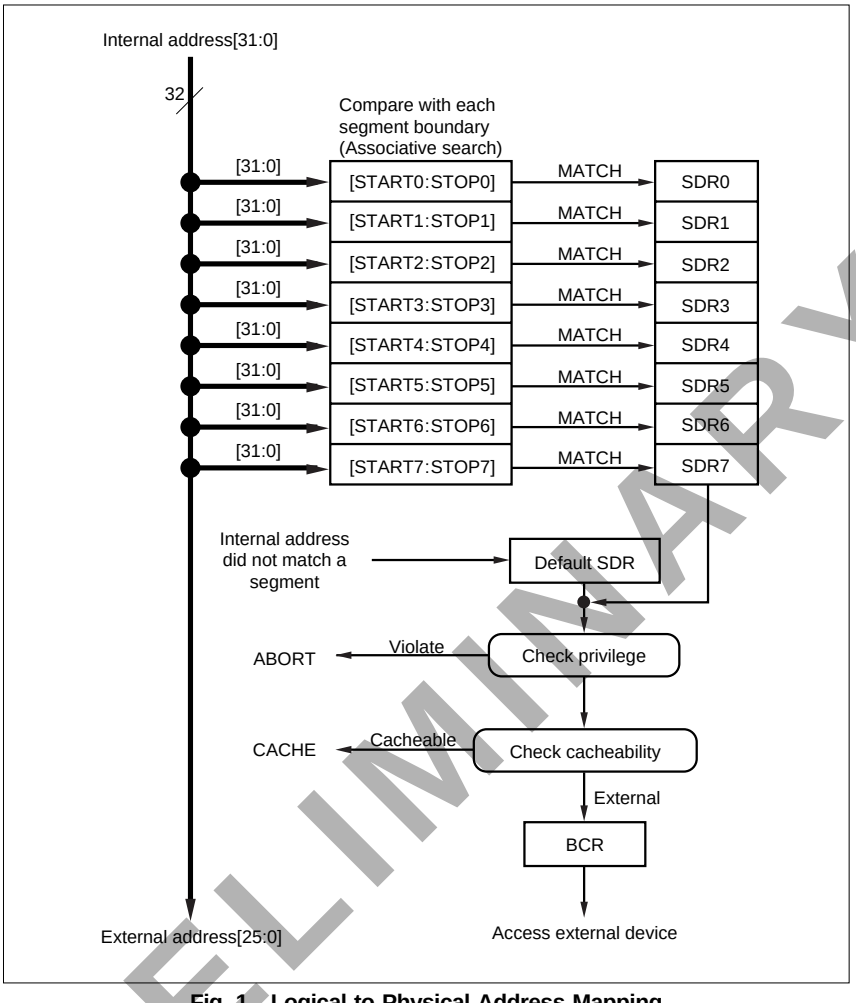


Fig. 1 Logical to Physical Address Mapping

DRAM Controller

The Embedded microcontroller supports a wide range of x 8 and x 16 DRAMs. The on-chip DRAM controller eliminates the need for an external DRAM controller, and simplifies the design of the system.

FEATURES

- Supports x 8 and x 16 DRAM
- Supports up to 2 banks
- Each bank can be programmed for :
  - Device size (256 kB to 64 MB)
  - Device width (8, 16 bits)
  - Fast page mode
  - Refresh rate (one RR for both banks)
  - Memory protection
- CAS before RAS refresh

UART

The Embedded microcontroller provides three 16C450-class UART macrocells (Universal Asynchronous Receiver/Transmitter). UART_0 supports a nine-wire interface (TxD, RxD, $\overline{RTS}$, $\overline{CTS}$, $\overline{DTR}$, $\overline{DSR}$, $\overline{DCD}$, $\overline{RI}$ and GND). UART_1 supports a six-wire interface (TxD, RxD, $\overline{RTS}$, $\overline{CTS}$, $\overline{RI}$ and GND). UART_2 supports a three-wire interface (TxD, RxD and GND) and is IrDA-IR and SHARP DASK-IR compliant.

FEATURES

- Double buffering
- 16-bit programmable baud rate generator
- Independently controlled interrupts
  - Receive, transmit, line status and MODEM status
- Fully-prioritized interrupt system control
- Programmable interface characteristics
  - 5 to 8-bit data
  - Even, odd, no parity
  - 1, 1-1/2, 2 stop bits
- Complete status reporting
- False start bit detection
- Line break generation and detection
- Full MODEM support on UART_0
- Loop back mode on UART_0
- UART_2 supports three modes of operation :
  - Pass through : Gives a total of three UARTs
  - IrDA SIR : Gives a total of two UARTs + one infrared Port
  - DASK SIR : Gives a total of two UARTs + one infrared port

Serial Infrared (SIR) Interface

The Embedded microcontroller has a serial infrared (SIR) interface that is IrDA and SHARP-DASK compatible. The interface connects to UART_2 and performs format encoding/decoding between UART format and IrDA/DASK SIR format. The SIR interfaces directly to any external IrDA/DASK transceiver module.

FEATURES

- IrDA SIR (version 1.0) compatible
- SHARP DASK SIR compatible
- Adds IR port to UART_2
- 2.4 kbps to 115.2 kbps IrDA data rate
- 2.4 kbps to 57.6 kbps DASK data rate
- Sleep mode to save power
- Three modes of operations :
  - Pass through : Three serial ports
  - IrDA SIR : Two serial ports + one infrared port
  - DASK SIR : Two serial ports + one infrared port
- UART format ↔ SIR format

APPLICATIONS

The SIR interface is an important feature that allows wireless communications and data exchange between hand-held devices, office equipment and office networks. It is an ideal solution for compact, low-power, cost-sensitive applications.

Pulse Width Modulator (PWM)

The Embedded microcontroller supports three fully independent pulse width modulator channels (PWM0, PWM1, PWM2) with the frequency range shown in Table 1.

Table 1 PWM Channels

SYSTEM CLOCK FREQUENCY	PWM PULSE FREQUENCY RANGE	
	16-BIT RESOLUTION	8-BIT RESOLUTION
16.7 MHz	4.10 Hz - 4.17 MHz or DC	1.05 kHz - 4.17 MHz or DC
25 MHz	6.15 Hz - 6.25 MHz or DC	1.58 kHz - 6.25 MHz or DC

FEATURES

- Each PWM channel is independent
- Frequency range :
  - DC High or Low
  - 4.10 Hz : 6.25 MHz
- Easy to program
- One 16-bit resolution PWM and two 8-bit resolution PWMs
- Programmable synchronous mode support
  - This will produce a synchronized sequence of PWM pulses
- Programmable pulse width (Duty Cycle) and interval (frequency)
  - Static programming : PWM is stopped/disabled
  - Dynamic programming : PWM is running/enabled
    - Double buffering allows dynamic programming
    - Updates to duty cycle and frequency are done at the end of a PWM cycle
- Enable/disable PWM
  - Disable PWM output at the end of a PWM cycle
- Sleep mode to save power
- PWM output connected to on-chip counters
  - This feature simplifies building applications like A/D
- Ability to invert the PWM output on the fly

APPLICATIONS

Pulse Width Modulation (PWM) is used in a variety of applications, such as :

- LED intensity control
- LCD gain and contrast
- Automotive engine control
- DC motor speed
- D/A and A/D conversion
- Sound synthesis
- Laser applications
- Servo motor control

LCD Controller

The LCD controller provides control and pixel data for directly driving LCD displays. The video frame buffer resides in the CPU main memory, eliminating the need for additional pins for a frame buffer memory interface and memory component(s) for the buffer. The LCD controller supports two primary modes : Binary mode (On, Off) and gray mode (On, Off or two gray shades).

FEATURES

- Frame buffer resides in CPU main memory
- LCD Display modes :
  - Binary mode : Pixels are On or Off (1 bit/pixel)
  - Gray mode : Pixels are On, Off or one of two intermediate gray shades (2 bits/pixel)
- LCD panel :
  - Single (4-bit and 8-bit data transfer)
  - Double (4-bit data transfer)
- Panel division or OR function in single panel mode
- Maximum resolution :
  - Horizontal : 2 048 pixels in binary mode, 1 024 pixels in gray mode
  - Vertical : 1 024 lines in single scan, 2 048 lines in dual scan
- Virtual display screen
- Smooth vertical scrolling
- DMA data transfers for panel refresh from main memory to maximize system performance
  - CPU can be running out of cache with no interference from the LCD controller

Counter/Timer

The Embedded microcontroller provides three independent 16-bit counter/timer (CNT/TMR) channels. Each channel can operate in one of six modes and works with either binary or BCD counting. The current counter value, control word, and current state of each OUT signal are available to the CPU.

FEATURES

- Six modes of operation :
  - Mode 0 : Interrupt on terminal count
  - Mode 1 : Hardware retriggerable one-shot
  - Mode 2 : Rate generator
  - Mode 3 : Square wave mode
  - Mode 4 : Software triggered strobe
  - Mode 5 : Hardware triggered strobe
- Binary or BCD counting
- CPU has access to the following :
  - Current counter value
  - Control word
  - Current state of OUT signals
- Selectable input clock
  - System clock
  - External clock
- Power management
  - Scale down system clock
  - Halt input clock

APPLICATIONS

- Accurate time delays
- Real time clock
- Event counter
- Digital one-shot
- Programmable rate generator
- Square wave generator
- Binary rate multiplier
- Complex waveform generator
- Motor control

Programmable Peripheral Interface (PPI)

The Embedded microcontroller provides an 8 225-class Programmable Peripheral Interface (PPI). It is a general-purpose I/O unit to interface peripherals to the Embedded microcontroller with no external glue logic. It has three 8-bit ports which can be programmed as inputs or outputs. The inputs and outputs can be read or written directly, or they can be strobed by external signals providing handshaking and interrupt signals.

FEATURES

- 24 programmable I/O signals
  - Three 8-bit ports : Port A, port B and port C
- Bit set/reset capability
- Read/write control register
- Three modes of operation
  - Basic input/output
  - Strobed input/output
  - Strobed bidirectional I/O
- Data, control and status bits

APPLICATIONS

The Programmable Peripheral Interface (PPI) can be used for :

- Printer interface
- Keyboard and display interface
- D/A and A/D interface
- Basic floppy disk interface

Interrupt Controller

The on-chip interrupt controller supports both internal and external interrupt sources. Internally there are six peripheral interrupt sources (three UARTs and three counters/timers). Externally there are six interrupt sources (INT[5:0]).

FEATURES

- Each interrupt source is programmable :
  - Enabled
  - Cleared
  - Active High or Low
  - Drive $\overline{\text{IRQ}}$ or $\overline{\text{FIQ}}$ (ARM7D Interrupts)
  - Level or edge triggered
- In sleep mode, the CPU clock is restarted when an interrupt is detected

Clock and Power Management

The clock and power management unit (C&PM) distributes the clock to the CPU core and peripherals, and provides a programmable clock divider to the CPU and peripherals that serves to reduce power. The CPU and peripheral can have their clocks stopped to further reduce power. The CPU clock, when halted, restarts at the fastest speed when an interrupt to the CPU is detected (either IRQ or FIQ).

FEATURES

- Clock control and power management
- Provide clocks to the CPU core and peripherals
- Provide a programmable clock divider to the CPU
- Provide a programmable clock dividers to UARTs and counter/timer (LCD controller and PWMs have built-In programmable clock dividers)
- Stop clocks to CPU and/or peripherals
- CPU clock is restarted when an interrupt is detected

Watchdog Timer

The watchdog timer is a hardware protection against malfunctions. It is a programmable timer that is reset by the software at regular intervals. Failure to do so causes the Embedded microcontroller to interrupt/reset. As long as the system is operating properly, the software that is executing clears the timer on a regular basis.

FEATURES

- Selectable input clock
  - System clock
  - System clock/8
- Selectable timeout interval
  - Four intervals
- Freeze option
- Protection mechanism
- Selectable timeout action
  - Non-maskable interrupt
  - Chip reset
- Power management

I/O Configuration

The Embedded microcontroller has a 24-bit input/output configuration register (IOCR) that allows the system designer to program multifunctional pins, selects between internal and external clocks for the UARTs and counter/timer, and controls the GATE signals to the counter/timer.

Reset

The Embedded microcontroller uses the **RESETI** input signal to generate a global chip reset. This signal must be held Low upon system power-up and remain Low for at least six clock cycles after V_{CC} has stabilized. **RESETI** is a level sensitive signal. A Low level causes the instruction being executed to terminate abnormally. When **RESETI** becomes High for at least one clock, the ARM CPU restarts from address 0 in supervisor mode and all peripherals are reset. During the Low period, the processor performs dummy instruction fetches with the address incrementing from the point where reset was activated.

In addition to holding the **RESETI** Low, the boundary scan reset input **TRST** must be pulsed or driven Low to achieve normal device operation upon power-up. If the boundary scan interface is used, then **TRST** must first be driven Low, then High. If the boundary scan interface is not used, then **TRST** input may be tied permanently Low.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{CC}	−0.3 to 6.0	V
Input voltage	V_{IN}	−0.3 to V_{CC}+0.3	V
Output voltage	V_{OUT}	−0.3 to V_{CC}+0.3	V
Operating temperature	T_{OPR}	0 to 70	°C
Storage temperature	T_{STG}	−40 to 125	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage	V_{CC}	3.0 to 3.6	3.3/5.0	4.5 to 5.5	V	1
Input High voltage	V_{IH}	2.0		V_{CC}+0.3	V	1
Input Low voltage	V_{IL}	−0.3		0.8	V	1
Operating temperature	T_{OPR}	0		+70	°C	

NOTE :

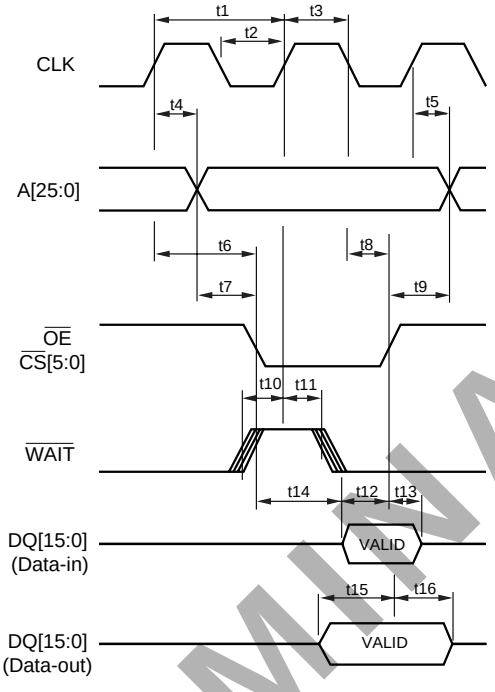
1. The applicable voltage on any pin with respect to V_{SS} (0 V).

DC ELECTRICAL SPECIFICATIONS

(T_{OPR} = 0 to +70°C)

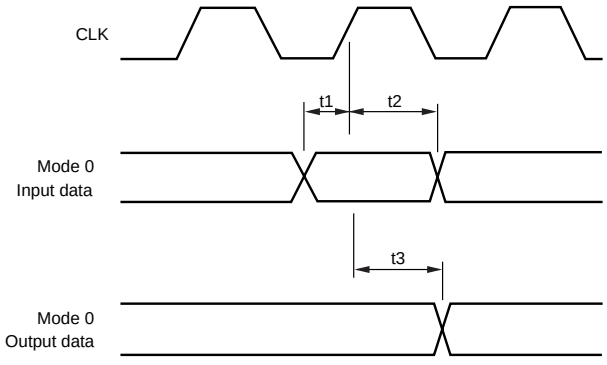
PARAMETER	SYMBOL	CONDITIONS	V_{CC} = 3.0 to 3.6 V		V_{CC} = 4.5 to 5.5 V		UNIT
			MIN.	MAX.	MIN.	MAX.	
Input Low voltage	V_{IL}		−0.3	0.8	−0.3	0.8	V
Input High voltage	V_{IH}		2.0	V_{CC}+0.3	2.0	V_{CC}+0.3	V
Output Low current	I_{OL}	V_{OL} = 0.4 V	2.0		8.0		mA
Output High current	I_{OH}	V_{OH} = 2.4 V	−4.0		−8.0		mA
Input leakage current	I_{IL}	V_{IN} = 0 to V_{CC} MAX.	–2	2	–2	2	µA
Output, input/output leakage current	I_{OZ}	V_{IN} = 0 to V_{CC} MAX.	–2	2	–2	2	µA
Average active operating current	I_{CC} (Active)	F = $F_{MAX.}$		30		70	mA
Average halt current	I_{CC} (Halt)	F = $F_{MAX.}$		1		2	mA

AC SPECIFICATIONS
• Memory I/F Timing



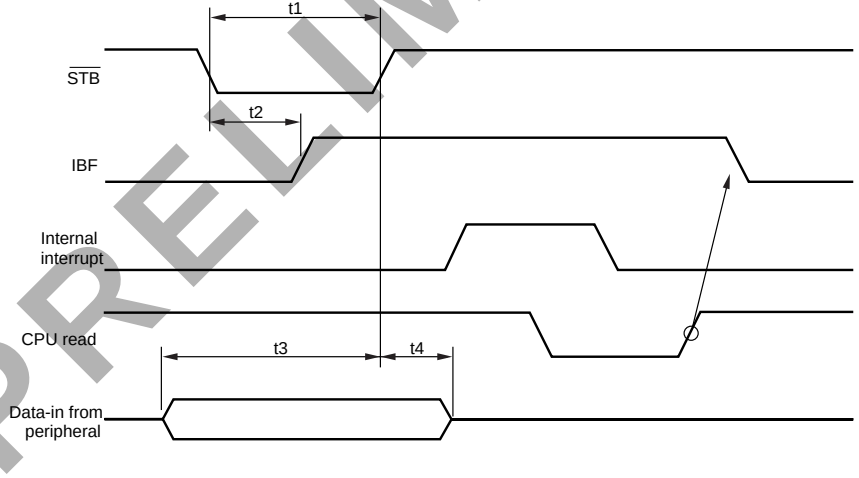
PIN NO.	DESCRIPTION	At 3.3 V		At 5.0 V		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_1	Clock period			40		ns
t_2	Clock High			20		ns
t_3	Clock Low			20		ns
t_4	Clock High to address valid				15	ns
t_5	Address hold from clock			5		ns
t_6	Clock High to control active - $\overline{WR}$, $\overline{OE}$, $\overline{CE}$ (5:0)				15	ns
t_7	Address to control setup			3		ns
t_8	Clock Low to control inactive - $\overline{WR}$, $\overline{OE}$, $\overline{CE}$ (5:0)			5	15	ns
t_9	Address hold from control inactive			3		ns
t_{10}	$\overline{WAIT}$ setup to clock High			5		ns
t_{11}	$\overline{WAIT}$ hold from clock High			5		ns
t_{12}	Data-in setup to control inactive - $\overline{WR}$, $\overline{CE}$ (5:0)			5		ns
t_{13}	Data-in hold from control inactive - $\overline{WR}$, $\overline{CE}$ (5:0)			0		ns
t_{14}	Control active to data-in valid - (memory access time)			25		ns
t_{15}	Data-out setup to control inactive - $\overline{WR}$, $\overline{CE}$ (5:0)			20		ns
t_{16}	Data-out hold from control ($\overline{WR}$, $\overline{CE}$ (5:0))			5		ns

• Parallel I/O Port Timing - Mode 0 Input & Output



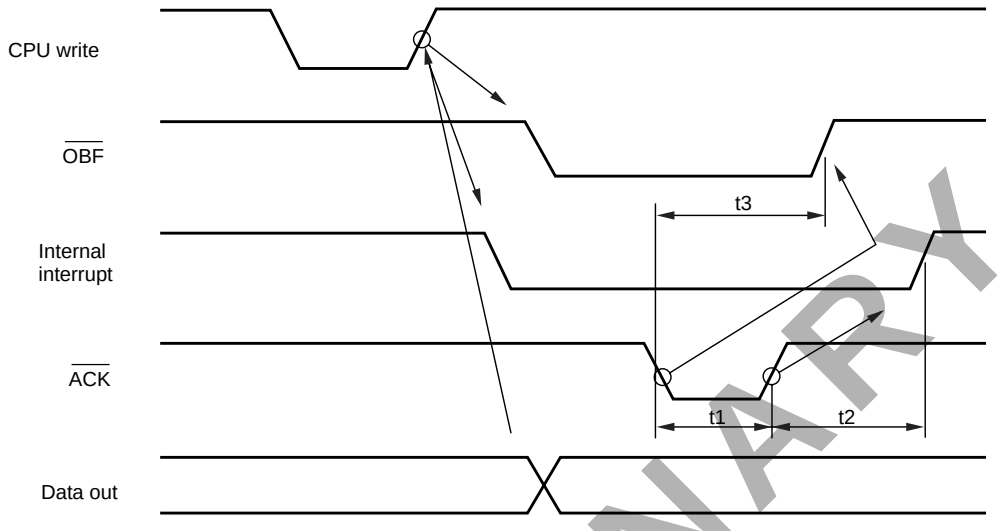
PIN NO.	DESCRIPTION	At 3.3 V		At 5.0 V		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_1	Data-in set-up to CLK	12		7		ns
t_2	Data-in hold from CLK	0		0		ns
t_3	CLK to data-out valid		34		20	ns

• Parallel I/O Port Timing - Mode 1 Strobed Input



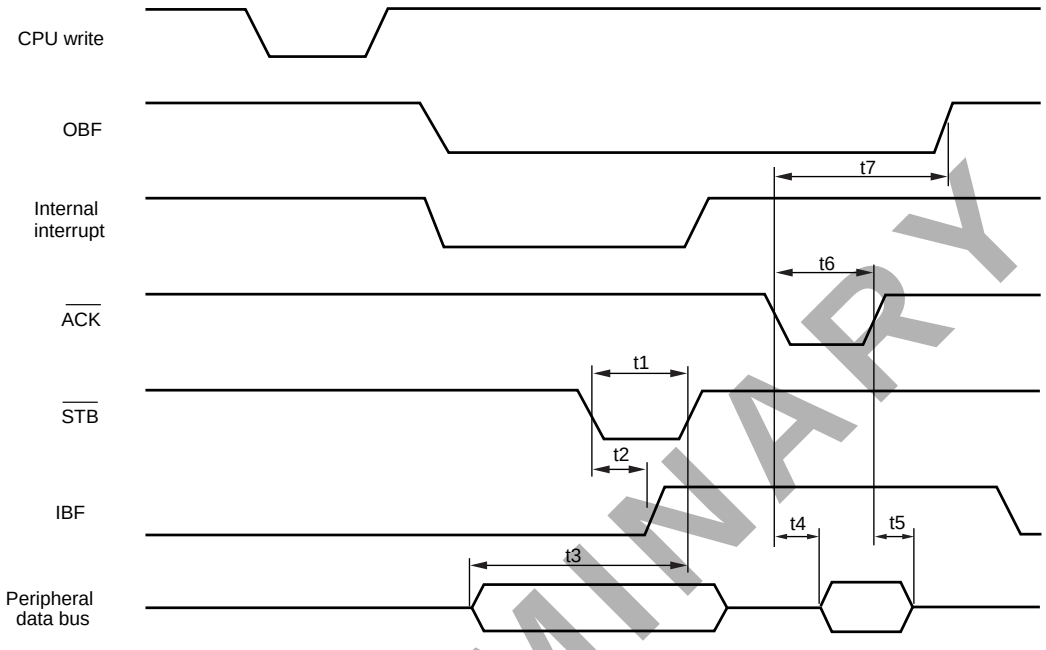
PIN NO.	DESCRIPTION	At 3.3 V		At 5.0 V		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_1	$\overline{STB}$ pulse width	45		25		ns
t_2	$\overline{STB}$ falling edge to IBF active	0	35	0	20	ns
t_3	Peripheral data-in set-up to $\overline{STB}$ High	20		10		ns
t_4	Peripheral data-in hold from $\overline{STB}$ High	0		0		ns

• Parallel I/O Port Timing - Mode 1 Strobed Output



PIN NO.	DESCRIPTION	At 3.3 V		At 5.0 V		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_1	$\overline{ACK}$ pulse width	40		25		ns
t_2	$\overline{ACK}$ High to interrupt disable	TBD		TBD		ns
t_3	$\overline{ACK}$ Low to $\overline{OBF}$ High delay		35		20	ns

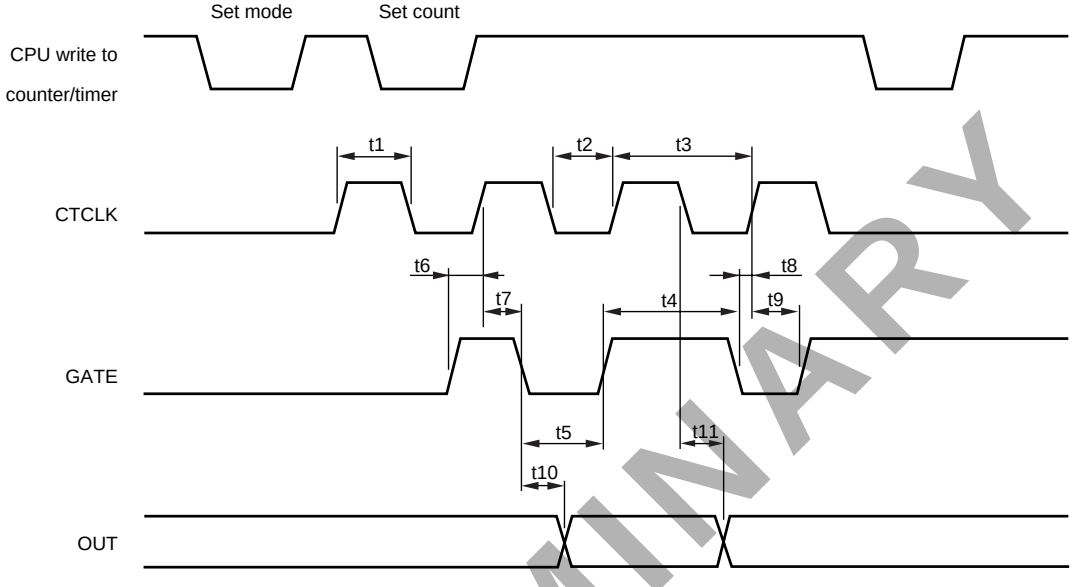
• Parallel I/O Port Timing - Mode 2 Bi-Directional Data Transfer



PIN NO.	DESCRIPTION	At 3.3 V		At 5.0 V		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_1	$\overline{STB}$ pulse width	40		25		ns
t_2	$\overline{STB}$ Low to IBF High delay		35		20	ns
t_3	Peripheral data-in set-up to $\overline{STB}$ High	20		10		ns
t_4	$\overline{ACK}$ Low to data-out valid delay		35		20	ns
t_5	$\overline{ACK}$ High to data-out Hi-Z delay		35		20	ns
t_6	$\overline{ACK}$ pulse width	40		25		ns
t_7	$\overline{ACK}$ Low to $\overline{OBF}$ High delay		35		20	ns

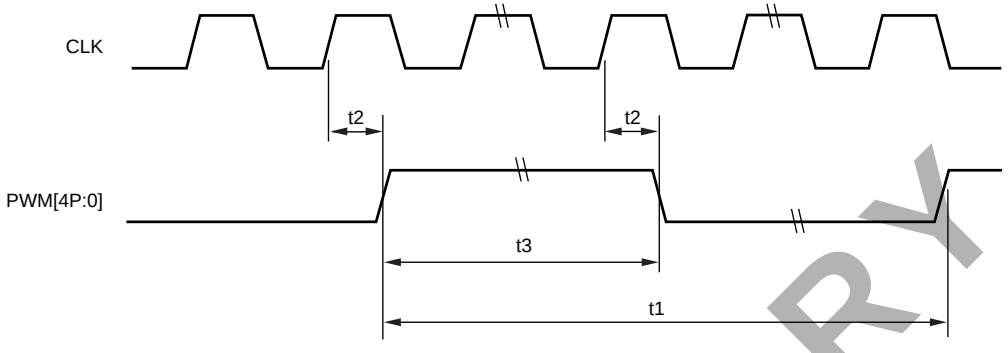
Hi-Z = High impedance

• Counter/Timer Timing



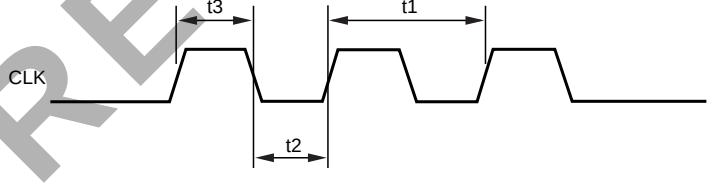
PIN NO.	DESCRIPTION	At 3.3 V		At 5.0 V		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_1	CTCLK High time	30		20		ns
t_2	CTCLK Low time	30		20		ns
t_3	CTCLK period	60		40		ns
t_4	GATE High time	40		25		ns
t_5	GATE Low time	40		25		ns
t_6	GATE High set-up to CLTCLK	15		10		ns
t_7	GATE High hold from CTCLK	0		0		ns
t_8	GATE Low set-up to CTCLK	15		10		ns
t_9	GATE Low hold from CTCLK	0		0		ns
t_{10}	GATE to OUT delay	0	35	0	20	ns
t_{11}	CTCLK to OUT delay	0	35	0	20	ns

• PWM Timing



PIN NO.	DESCRIPTION	At 3.3 V		At 5.0 V		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_1	PWM pulse period	CLK/ prescale		CLK/ prescale		CLK periods
t_2	CLK to PWM delay	0	15	0	12	ns
t_3	PWM active pulse width		34		20	CLK periods

• Clock Timing

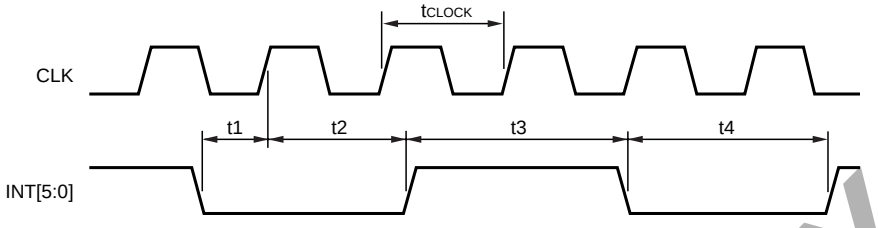


PIN NO.	DESCRIPTION	At 3.3 V		At 5.0 V		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_1	Clock cycle time	60		50		ns
t_2	Clock Low time	24		20		ns
t_3	Clock High time	24		20		ns

NOTE :

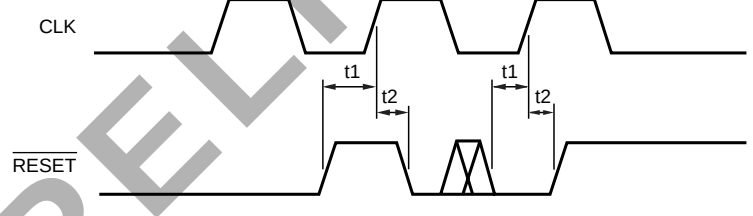
CLK timings are measured to 50% V_{CC}.

• External Interrupt Timing



PIN NO.	DESCRIPTION	At 3.3 V		At 5.0 V		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_1	External interrupt set-up time. (only used to insure capture on next active clock edge)	20		10		ns
t_2	External interrupt hold time. (only used to insure capture on next active clock edge)	20		10		ns
t_3	External interrupt active High interval	3 x t_{CLOCK}		3 x t_{CLOCK}		ns
t_4	External interrupt active Low interval	3 x t_{CLOCK}		3 x t_{CLOCK}		ns

• Reset Timing



PIN NO.	DESCRIPTION	At 3.3 V		At 5.0 V		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
t_1	$\overline{\text{RESET}}$ setup to CLK	60		50		ns	1, 2
t_2	$\overline{\text{RESET}}$ setup to CLK	24		20		ns	1, 2

NOTES :

1. $\overline{\text{RESET}}$ is an asynchronous input, setup and hold times only ensure the signals are captured at the specified clock edge.
2. $\overline{\text{RESET}}$ must remain Low for 16 CLK periods after the power supply and clock have stabilized.

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